E-tec Interconnect
Industrial Zone C,
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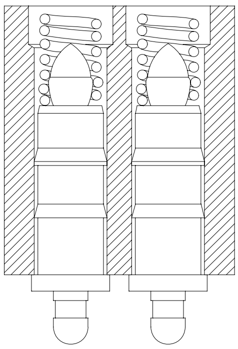
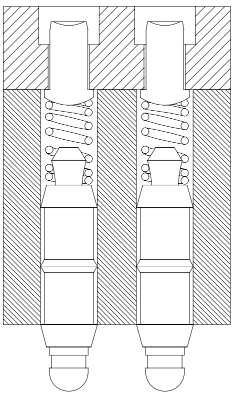
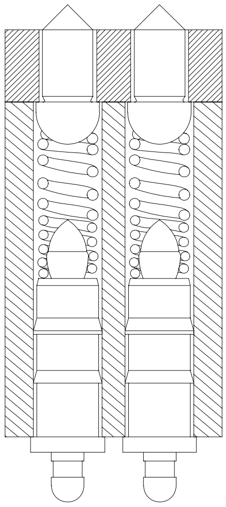
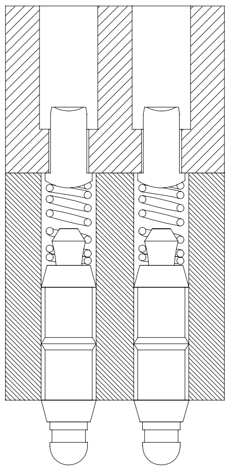
Patented socketing system for the BGA/CSP technology

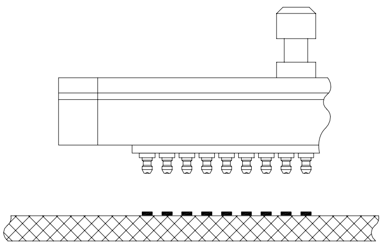
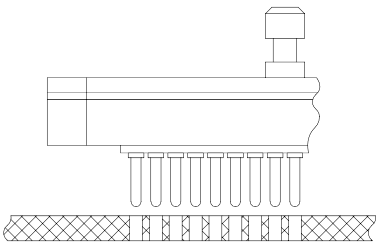
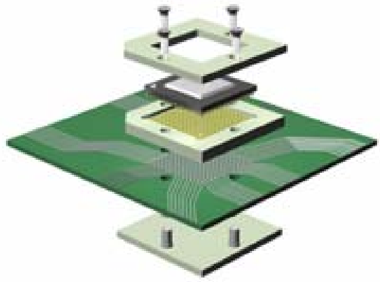
Features:

- ZIF handling & only 40 grams per contact after closing the socket
- Sockets adapt to all package styles (at present down to 0.50mm pitch):
  Ceramic & plastic BGA (cavity up & down), CSP, LGA, CGA, PSGA
- Same PCB layout as the chip (no holes required for SMD socket)
- Raised SMD for lifting socket over components
- Thermal expansion, shock & vibration absorbed by E-tec contact design
- Low profile socket (standard twist lock is less than 10mm with chip)
- Heat dissipation with open frame or heatsinks
- Low inductance of less than 2 nH
- Frequency range up to 3 Ghz
- LGA contact design can also be used for board-to-board connections

Available contact designs:

BGA ball grid array contact design *(patented)* **(standard size solderballs)**	BGA ball grid array contact design *(patented)* **(small size solderballs)**	LGA land grid array contact design *(patented)*	CGA Column grid contact design *(patented)*
			

Available socket styles:

SMT style	Through-hole style	"compression type"
		

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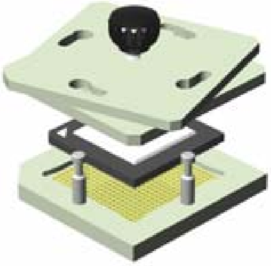
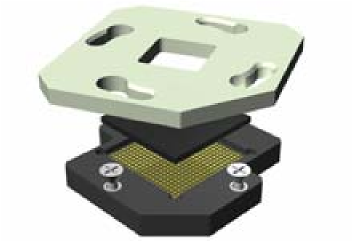
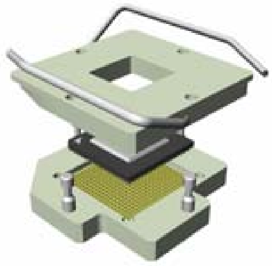
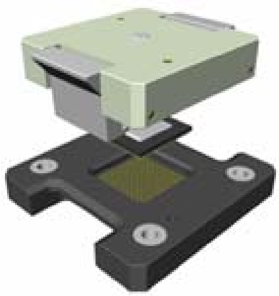
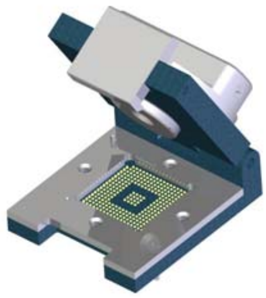
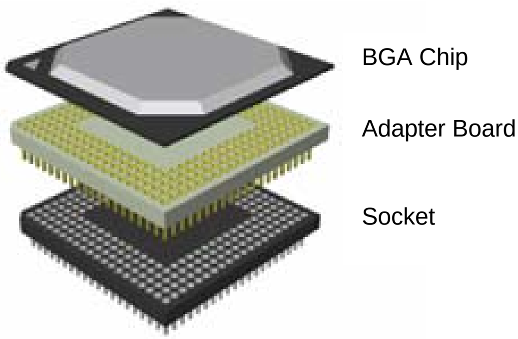
Available retention designs:

"Knob lock" for multiple insertions and extractions of chips, for example in test and burn-in 	"Twist lock" for prototypes and pre-production 	"ZIF (lever) lock" for pre-production and volume productions 
"Quick lock" for test purposes (socket up to 80 pins) 	"Quick lock" for test purposes (socket as of 81 pins) 	"Clamshell" for test purposes 
Other socket styles: Please contact E-tec for other socket styles or custom specials		

Alternative to E-tec BGA socket = E-tec Adapter system:

Advantages: smaller outer dimensions than true socket

Disadvantages: Chip needs to be soldered to adapter board
Can only be used with BGA chips
Smallest pitch is 1.00mm
Relatively high insertion & extraction forces (difficult without tool)

BGA Adapter Socket system	Extraction tool for adapter system
	

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Classification Reflow Profiles as per IPC/JEDEC J-STD-20C

Table 5-2 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3 °C/second max.	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)	 183 °C 60-150 seconds	 217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	See Table 4.1	See Table 4.2
Time within 5 °C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

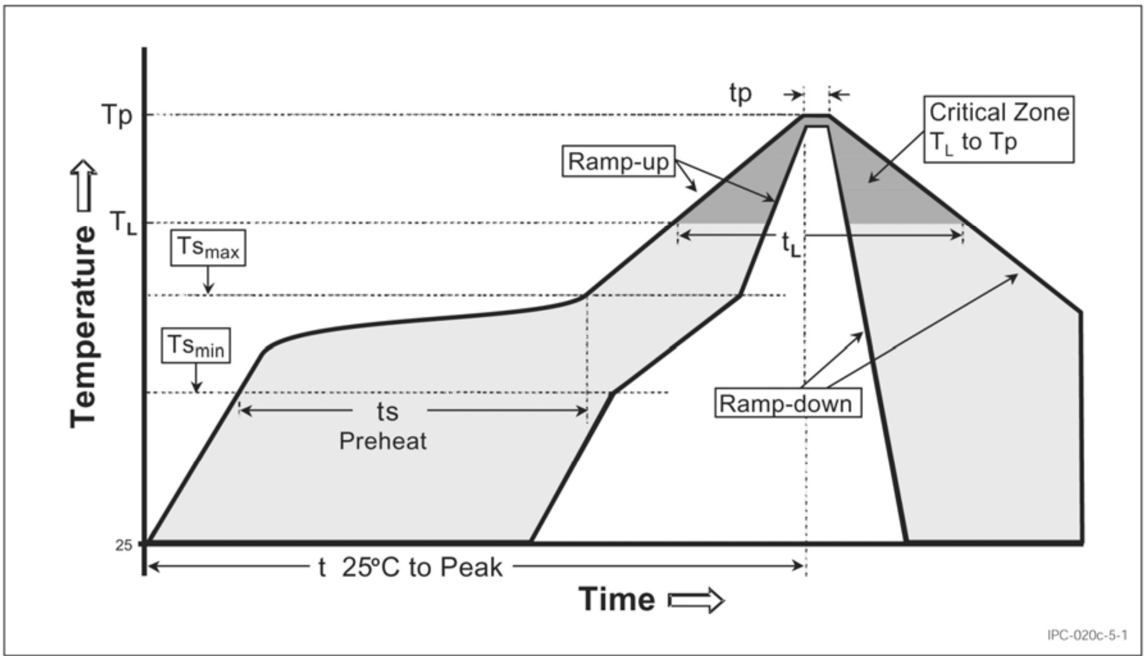

Figure 5-1 Classification Reflow Profile

Table 4-1 SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm³ <350	Volume mm³ ≥ 350
<2.5 mm	240 +0/-5 °C	225 +0/-5°C
≥ 2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 4-2 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6 mm	260 +0 °C *	260 +0 °C *	260 +0 °C *
1.6 mm - 2.5 mm	260 +0 °C *	250 +0 °C *	245 +0 °C *
≥2.5 mm	250 +0 °C *	245 +0 °C *	245 +0 °C *
* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0 °C. For example 260 °C+0°C) at the rated MSL level.			

Note 1: The profiling tolerance is + 0 °C, -X °C (based on machine variation capability) whatever is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 4.2.

Note 2: Package volume excludes external terminals (balls, bumps, lands, leads) and/or nonintegral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Note 4: Components intended for use in a "lead-free" assembly process **shall** be evaluated using the "lead free" classification temperatures and profiles defined in Tables 4-1, 4.2 and 5-2 whether or not lead free.

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Chip package styles used with E-tec sockets:

BGA "Ball Grid Array"

Comprises plastic packages with "cavity up" (= processor is located on top of the substrate) and "cavity down" (= processor is located below the substrate), as well as ceramic packages. The plastic packages with 1.27mm ball pitch have solderballs of 0.60mm (.024 inch) height with a diameter of 0.76mm (.030 inch), while the ceramic packages have solderballs of 0.90mm (.035 inch) height with a diameter of 0.86 (.034 inch). The most common pitch is 1.27mm (.050 inch), but other pitches such as 1.00mm (.039 inch), 1.50mm (.059 inch) or 2.00mm (.079 inch) or interstitial pitches are also available.

CSP "Chip Scale Packaging"

The outer dimensions of these packages, which are also supplied in "ball grid array technology", are designed so as not to exceed the size of the processor by more than 20%. The pitch starts with 0.80mm (.032 inch) and reduces to 0.50mm (.020 inch). The solderball diameter in this pitch size is as little as 0.30mm (.012 inch).

LGA "Land Grid Array"

These chips are supplied with a gold pad (= land) instead of the solderballs. The advantage of this package is that it is cheaper to manufacture (no solder balls required). The disadvantage is that it is more difficult to assemble onto a PCB (connector required).

CGA "Column Grid Array"

Soldercolumns of more than 2.00mm (.079 inch) height replace the standard 0.90mm (.035 inch) solderballs. These soldercolumns overcome the problem of "thermal expansion" of the chip and the inherent mechanical stress this exercises on the solderjoints of standard solderballs. These relatively soft columns have the ability of absorbing the "micro movements" of the chip thus eliminating the problem.

QFN/MLF "micro leadframe"

These chips are a near CSP plastic encapsulated packages which present lands instead of solderballs around the four sides of the package.